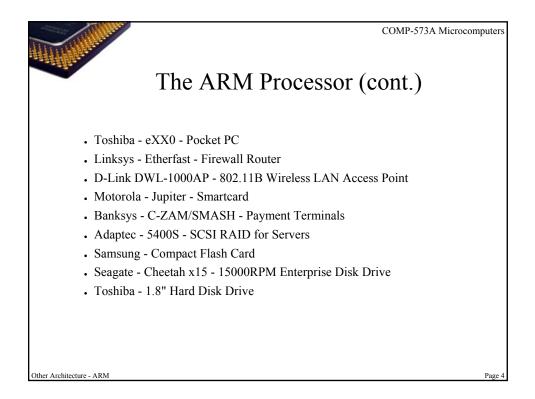
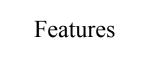


Other Architecture - ARM

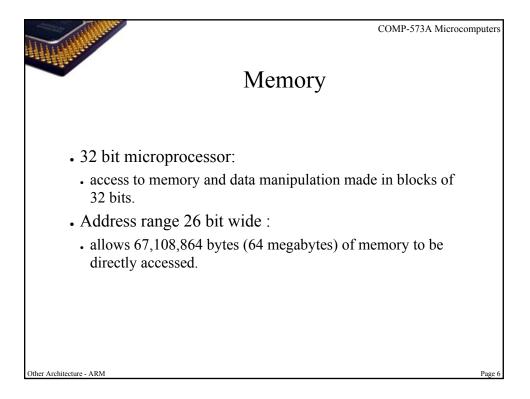


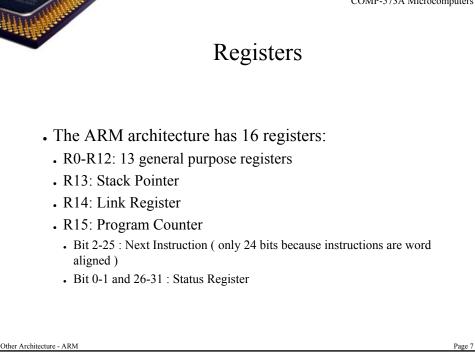


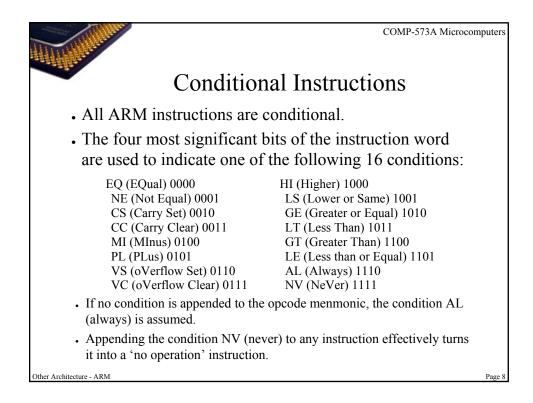
• RISC Architecture

- Reduced instruction set only 25 basic instruction types.
- Most operations are executed over registers.
- All instructions can be conditional.
- Multiple addressing modes are provided (including modes that allow direct bit shifting)
- Manual stack manipulation
 - Stack addressing must be explicitly programmed
 - Subroutines (including return) must be explicitly programmed
- · Big-endian and little-endian

Other Architecture - ARM





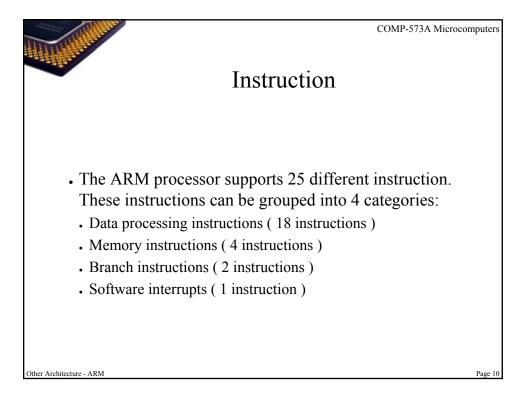


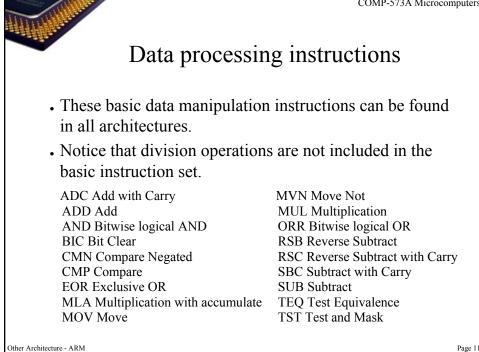


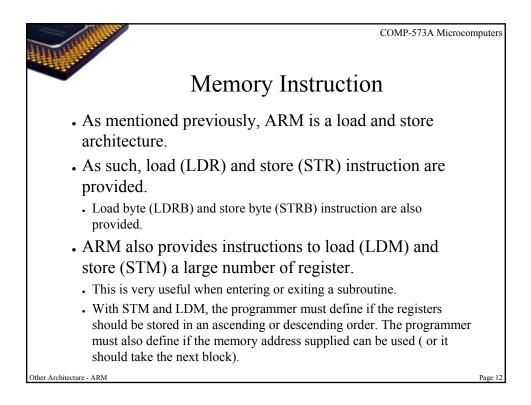
• The ARM architecture offers extensive support for memory stack by allowing programmers to chose one of four stack format/orientation.

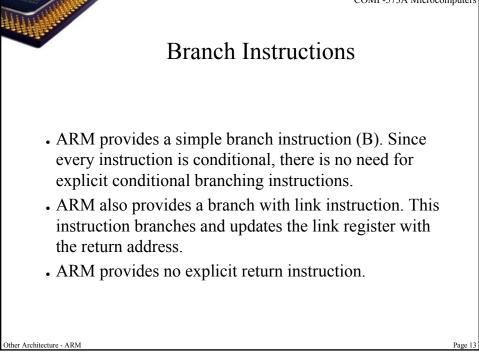
- Empty or Full:
 - · Empty: Stack Pointer points to the next free space on stack
 - Full: Stack Pointer points to the last item on the stack
- · Ascending or Descending:
 - Ascending: Grows from low memory to high memory
 - · Descending: Grows from high memory to low memory
- I386, Sparc and PowerPC all use a *"Full, Descending"* stack format.

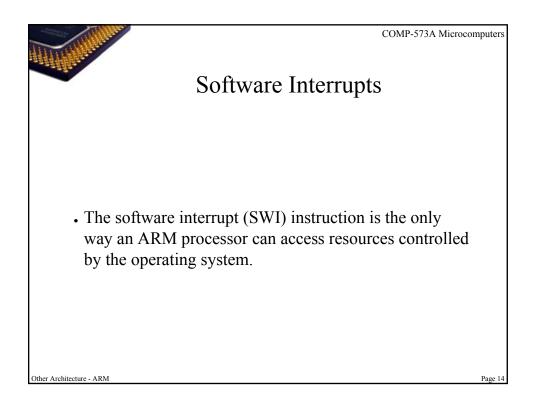
Other Architecture - ARM

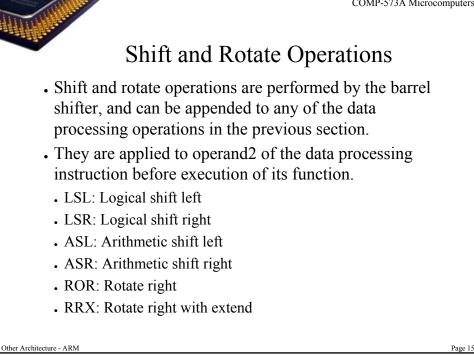


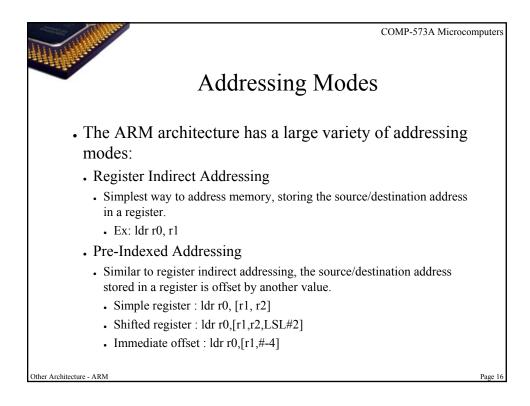


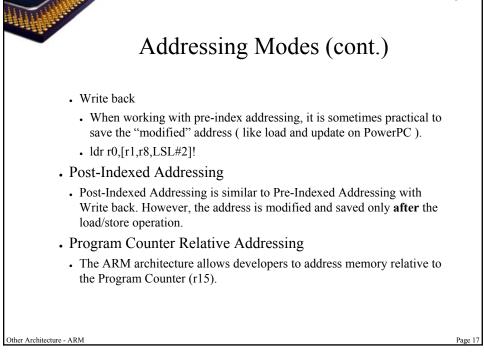


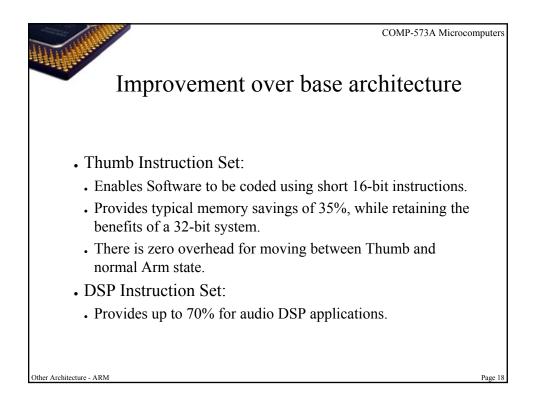


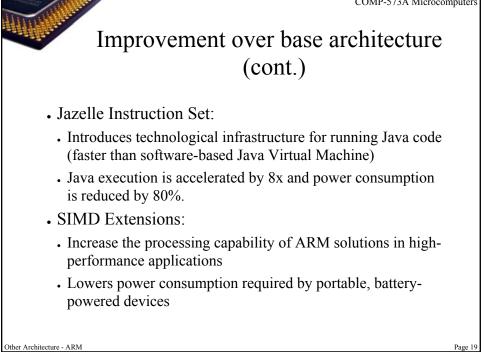


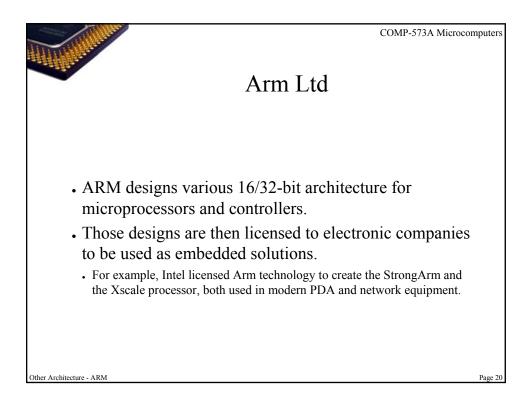


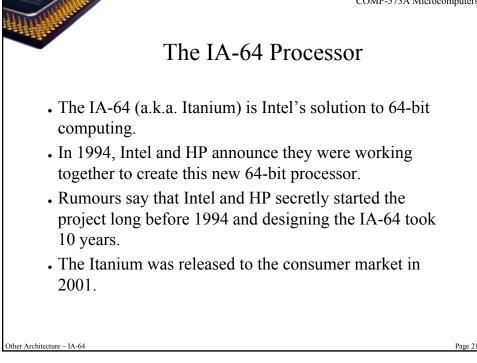


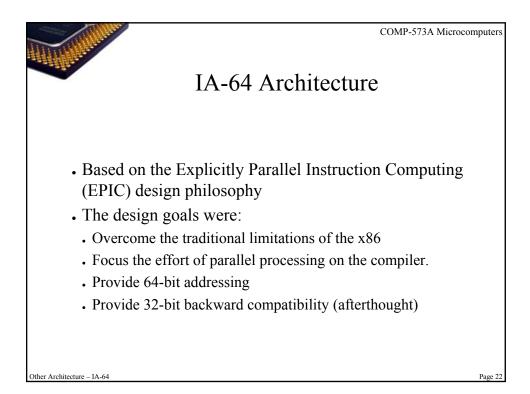


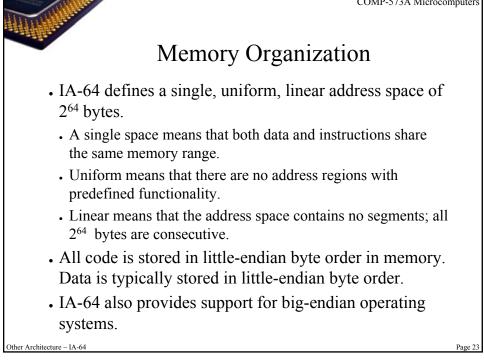


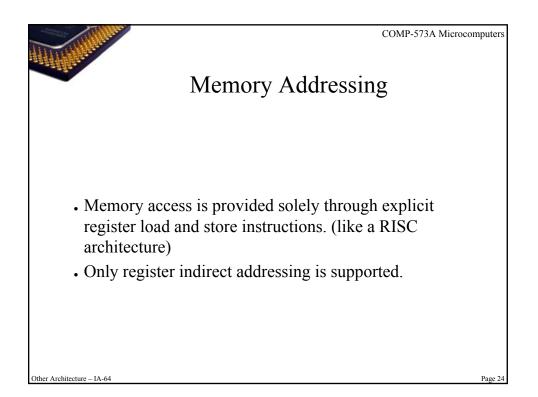


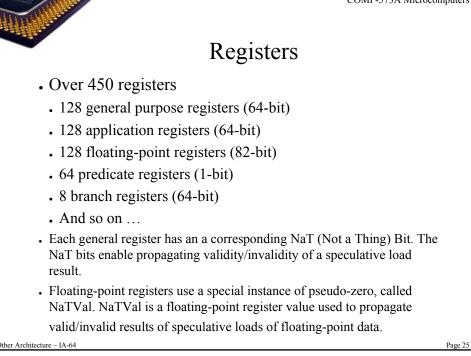


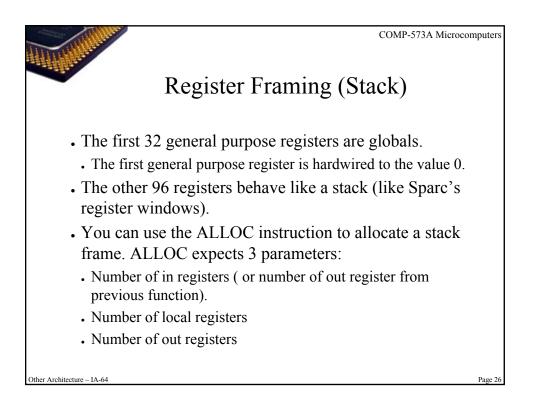




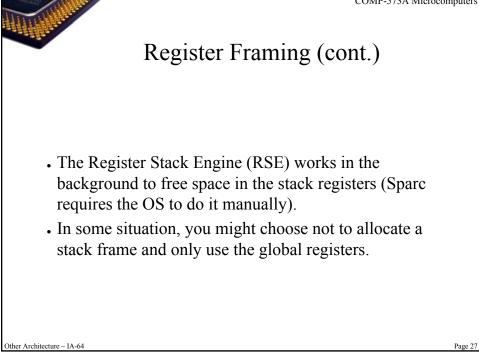


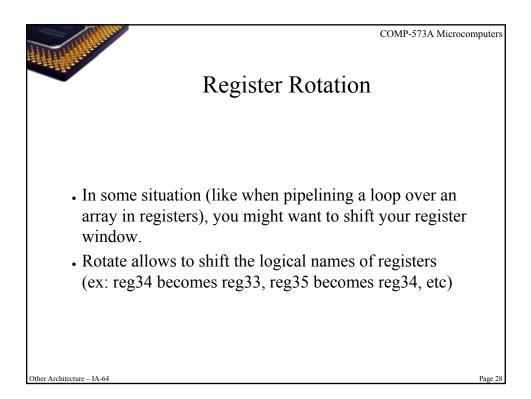




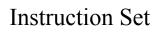








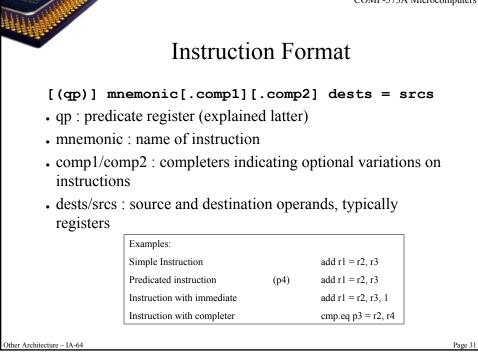
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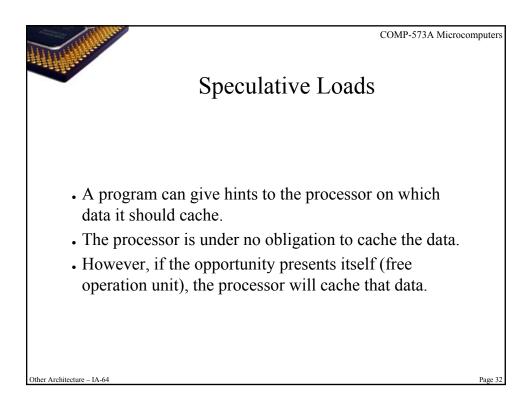


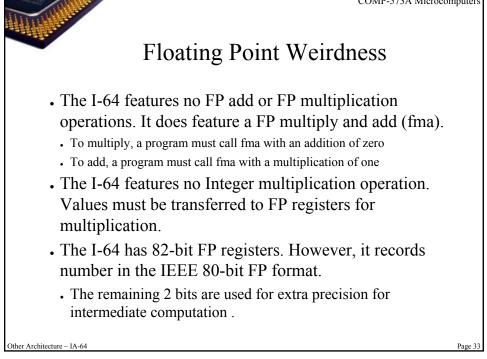
- Instructions in IA-64 are 41 bit in length.
 - Addressing a register requires 7 bits.
- Instructions are delivered to the execution unit in bundles of 128-bit.
 - That's 3 instructions and a 5-bit template.
- Instructions are clustered in groups. These groups are collections of instructions that can be dispatched simultaneously without dependencies or interlocks.
- Groups and bundles are **not** the same things.

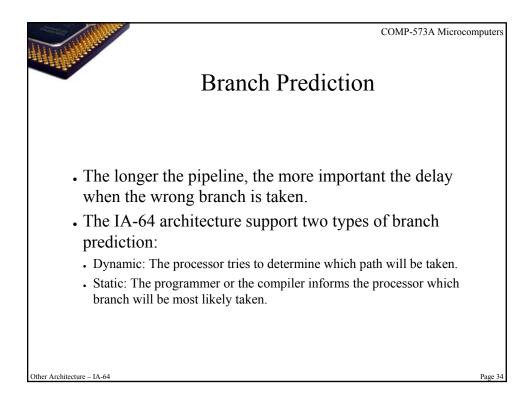
Other Architecture - IA-64

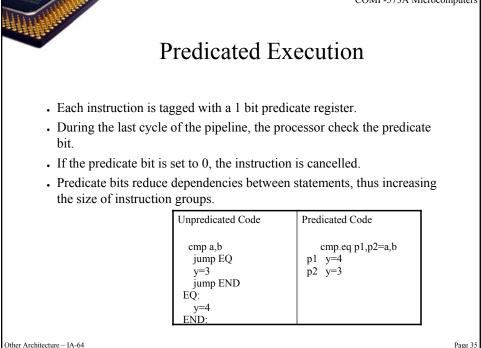
COMP-573A Microcomputers Instruction Set (Cont.) • It's the compilers job to determine which instructions can be grouped together (CPU does no checking). • All instructions are executed in order. • Instructions can be divided into 4 categories: integer, load/store, floating-point and branch operations. • IA-64 opcodes are not unique. They can be reuse up to 4 times (depending on the operation unit). • It's the job of the 5-bit template (in the bundle) to determine which unit should execute which instruction. • 5-bit is not enough to represent the 64 possible combinations different instructions could require • Intel provides 24 possible templates Other Architecture - IA-64 Page 30

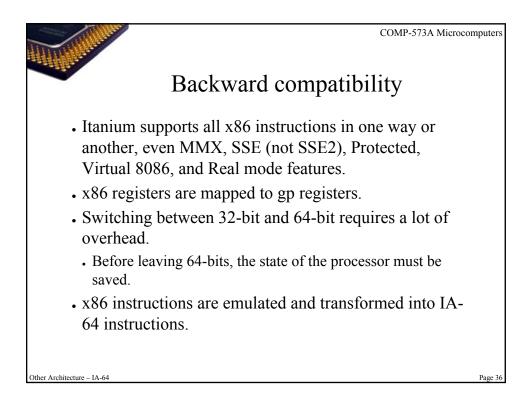


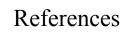












- ARM http://www.arm.com
- The ARM Microprocessor http://www.geocities.com/wonglinhoo/Arm.htm
- IA-64 Tutorials http://www.cs.nmsu.edu/~rvinyard/itanium/ia64wbts/
- 64-Bit CPUs: What You Need to Know http://www.extremetech.com/print_article/0,3428.a%253D22477.00.asp

Other Architecture - IA-64

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